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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,640	06/25/2003	Akimitsu Shimamura	28951.5292	1038

53067 7590 05/19/2006

STEPTOE & JOHNSON LLP
1330 CONNECTICUT AVE., NW
WASHINGTON, DC 20036

EXAMINER

TREAT, WILLIAM M

ART UNIT	PAPER NUMBER
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2181

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/602,640

Applicant(s)

SHIMAMURA

Examiner

William M. Treat

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. Claims 9-17 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Zaiki et al. (Patent No. 6,119,221).
4. Zaiki taught the invention of claim 9 including a semiconductor device comprising: an instruction memory storing for associating, with an address, an instruction program comprising a plurality of instruction codes, and storing therein such instruction program as data (col. 1, lines 14-35); an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes thereof (Fig. 1); a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal (Figs. 6(a) and Fig. 6(c)); and an execution block for executing an instruction according to a control signal outputted from the decode block (Figs. 6(a) and Fig. 6(c)), and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction (col. 13, lines 7-25), wherein when the instruction fetch block performs the fetch process, one of a branch address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected

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according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory (col. 11, lines 22-59).

5. As to claim 10, Zaiki taught the semiconductor device according to claim 9, wherein a branch address has a value obtained by adding a value of an address for reading out an instruction program and a value of displacement information included in such instruction program (col. 11, lines 22-59).

6. As to claim 11, Zaiki taught the semiconductor device according to claim 9, further comprising a conditional branch instruction determiner for determining whether or not a conditional branch instruction is present in an instruction code outputted from the instruction fetch block, wherein when the conditional branch instruction determiner detects a conditional branch instruction and outputs a signal indicating execution of such conditional branch instruction, address selection based on a conditional-branch-taken signal is performed, and when the conditional branch instruction determiner detects no conditional branch instruction, address selection based on such conditional-branch-taken signal is not performed (col. 11, lines 22-59).

7. The examiner has given little weight to the preamble to applicant's claim 9 since nothing recited in the body of the claim is in anyway related to semiconductors or semiconductor technology. However, the examiner considers it inherent in Zaiki that his invention would be a semiconductor device since he was discussing a general-purpose, pipelined, von Neumann processor which are fabricated today on semiconductor chips.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaiki et al. (Patent No. 6,119,221).

10. Should applicant chose to argue the term semiconductor device in claim 9 is more than merely the recitation of what is the recognized computer-industry standard for today's processors, the examiner takes Official Notice of the fact that fabrication of processors as taught by Zaiki is conventionally done as integrated circuits on semiconductor chips. The technology is so pervasive that one finds alternatives only in museums or research settings. Therefore, Zaiki would have been motivated to fabricate his processor as a semiconductor device because of readily available technology and expertise as well as the fact nothing else would be commercially viable. As to the other elements of applicant's claims 9-11, see paragraphs 4-6, *supra*.

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 12-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

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13. Claims 12-17 make reference to an “upper bit” and a “lower bit” and describe various attributes of them. The examiner can find nothing in the original disclosure to support such claim language. There are references in applicant’s original disclosure to “digits”, which consist of multiple bits, and “upper bits” and “lower bits” which might be consistent with some of what applicant is trying to claim, but applicant’s claims for the attributes of the “upper bit” and “lower bit” of addresses are new matter, as best the examiner can determine.

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. As applicant’s claims for the attributes of the “upper bit” and “lower bit” of addresses seem to be new matter, applicant seems to have failed to particularly point out and distinctly claim the subject matter which applicant regards as the invention. See paragraph 13, *supra*, for further explanation.

17. Applicant’s arguments with respect to claims 9-17 have been considered but are moot in view of the new ground(s) of rejection.

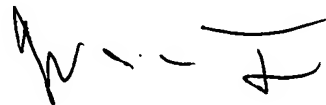
18. Applicant’s amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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19. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

20. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER